UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Offic
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/467,675	12/21/99	LIOU	F 252103-4540

DANIEL R MCCLURE
THOMAS KAYDEN HORSTEMEYER
& RISLEY LLP SUITE 1500
100 GALLERIA PARKWAY NW
ATLANTA GA 30339

MMC2/0813

EXAMINER	
NADAV,O	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/13/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/467,675	Applicant(s) Liou et al.
	Examiner ORI NADAV	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 20, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-16 and 18-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (6,118,154) in view of Hu et al. (6,121,077), Erdeljac et al. (5,554,873) and Japanese Patent #4-76959.

Yamaguchi et al. teach in figure 22 an ESD protection structure having a silicon sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad 30 and a node 71 and the internal circuit electrically connected to the node (figure 19), comprising a silicon resistor 36 formed over an insulating oxide material layer 2, electrically coupled between the input pad 30 and the node 71, and horizontally isolated by an isolation structure, at least a single crystal silicon sided P/N junction diode 34 formed over the insulating material layer 2, wherein the diode is electrically coupled between one terminal of a corresponding power supply 32 and a node 71.

Although Tamaguchi et al. do not explicitly state that resistor 36 is horizontally isolated, resistor 36 must be horizontally and vertically isolated in order not to short circuit the device. Therefore, Tamaguchi et al. teach horizontally isolated resistor, as claimed.
In the alternative, Erdeljac et al. teach in figure 11 a silicon resistor 34 formed over an insulating oxide material layer 20, and horizontally isolated by an isolation structure 38.
Japanese Patent #4-76959 teach in figure 1 a single crystal silicon resistor 15a-15d formed over an insulating oxide material layer 14, and horizontally isolated by an isolation structure 18.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to horizontally isolate the resistor of Yamaguchi et al.'s device in order to operate the device without short circuiting the elements of the device.
Yamaguchi et al. do not teach a silicon layer comprising monocrystalline silicon.
Hu et al. teach an ESD protection circuit having an SOI structure formed of monocrystalline silicon (column 1, line 27).
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a silicon layer comprising monocrystalline silicon in Yamaguchi et al.'s device because it is conventional in the art to form ESD protection device having an SOI structure of monocrystalline silicon in order to improve the performance of the device by the use of a monocrystalline silicon, of which judicial notice may be taken. Furthermore, the advantages of using a single crystal resistor

over a polycrystalline resistor are well known in the art. Note Japanese patent # 3-142868 is cited to support the well known position.

Regarding claims 4 and 10, Yamaguchi et al. teach an input buffer 37 electrically coupled between the node and the internal circuit.

Regarding claims 7 and 13, Yamaguchi et al. teach a diode comprising a MOS transistor formed over the insulating layer, wherein one of the source/drain regions electrically connects to a gate by a wire line.

Regarding claim 8, Yamaguchi et al. teach junction diodes comprising first and second diodes, electrically connected between the node and one terminal of a first and second power supply, respectively.

Regarding claim 9, Yamaguchi et al. teach in figure 10 an input resistor comprising a plurality of single resistors 64 formed over the insulating material layer, wherein each of the resistors is electrically coupled between the input pad and the node. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an input resistor comprising a plurality of single resistors in Yamaguchi et al.'s device in order to provide better protection for the device.

Regarding claim 14, Yamaguchi et al. teach in figure 22 first, second and third conductive layers 13, 14, 15 formed over the insulating layer and electrically connecting the resistor between the input and the integrated circuit and the diode to the integrated circuit, respectively.

Regarding claim 19, Yamaguchi et al. (figures 10 and 22, #11) and Hu et al. (figure 14) teach resistors isolated by an isolation structure.

Regarding claim 20, it is conventional to use STI as an isolation structure, of which judicial notice may be taken.

Response to Arguments

3. Applicant's arguments with respect to claims 1-16 and 18-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference N is cited as being related to a single crystal resistor.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Ori Nadav

August 3, 2001